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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/722,853	11/25/2003	Don T. Lam	1020.P16533	8556

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EXAMINER	
RUTLAND WALLIS, MICHAEL	
ART UNIT	**PAPER NUMBER**
2836	

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Please find below and/or attached an Office communication concerning this application or proceeding.

The time period for reply, if any, is set in the attached communication.

Office Action Summary	Application No.	Applicant(s)	
	10/722,853	LAM, DON T.	
	Examiner	Art Unit	
	Michael Rutland-Wallis	2836	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *20 June 2007*.

2a)☒ This action is **FINAL**. 2b)☐ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-20* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1-20* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☒ The drawing(s) filed on *25 November 2003* is/are: a)☒ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO/SB/08) Paper No(s)/Mail Date _____.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____.
5) ☐ Notice of Informal Patent Application
6) ☐ Other: _____.

DETAILED ACTION

Response to Arguments

Applicant's arguments with respect to claims 1-20 have been considered but are moot in view of the new grounds of rejection.

Claim Rejections - 35 USC § 103

The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

Claims 1-5, 7-11, 15-20 are rejected under 35 U.S.C. 103(a) as being unpatentable over Humpherys et al. (U.S. Pat. No 6,128,682) in view of Amicangioli et al. (U.S. Pat. No 6,327,242)

With respect to claims 1, 5, 15-16 and 19-20 Humpherys teaches an isolation circuit (see Fig. 2 and 3), comprising: a control circuit (control logic item 175 see col. 5 lines 20-25) to receive as input a power status signal (col. 5 lines 1-5) said control circuit to output a switch control signal (output signal to switch 180), said switch control signal to comprise a switch close signal if said power status is valid (switch closed normal operation), and a switch open signal if said power status is invalid (see col. 5 lines 20-25); and at least one switch (item 180) to connect to said control circuit, said switch to

receive said switch control signal and a component signal (carried in bus lines 77) and operate (open/close) in accordance with said switch control signal, wherein said isolation circuit is implemented as a part of a management module (configured to isolate management board item 55) within a shelf comprising a plurality of shelf components (see Fig. 2 circuitry on and in communication with the management board), with said switch to prevent communication of said component signal when said switch is in an open state and said component signal to be shared (via PCI bus lines) among shelf components communicating within said shelf through said management module when said switch (180) is in a closed state. Humpherys teaches isolating the component signal when the system host is unavailable however does not teach the use of a software signal to be received to signal the control circuit to isolate the component signal. Amicangioli teaches the use of a software timer opening of switch when a failure or expiry of a software timer (col. 4 lines 55-65) to increase the reliability of the network traffic processor deployment. It would have been obvious to one of ordinary skill in the art at the time of the invention to modify Humpherys to include a software input to the control circuit in order to increase the reliability of the network.

With respect to claim 2 Humpherys as modified by Amicangioli teaches said control circuit outputs said control signal in accordance with said software event signal (i.e. expiry of watchdog timer).

With respect to claim 3 Humpherys as modified by Amicangioli teaches said switch receives as input a software control signal (explicit signals passed via line 19),

and said switch switches between said open state and a closed state in accordance with said software control signal.

With respect to claim 4 Humpherys teaches a logic block with multiple bus lines entering the switch block, and while Humpherys is silent on the nature or number of the circuitry components contained with the block diagram disclosed in Humpherys. It would have been obvious to one of ordinary skill in the art at the time of the invention to modify Humpherys to use more than one switch circuit in the switching block in order to isolate all the bus lines entering from the PCI connector.

With respect to claim 7 Humpherys teaches A system, comprising: a bus (PCI bus both primary and secondary); a shelf having a plurality of shelf components (shelf with sever system 10); a management module (55) to connect to said bus, said management module to manage a plurality of component signals communicated between said shelf components; an wherein said management module comprises an isolation circuit (detailed in Fig. 3) to isolate said shelf component signals upon detection of a power interruption (col. 5 lines 1-5) from a power supply (not shown) to one of said shelf components, and said component signal is shared among shelf components communicating within said shelf through said management module when there is no detection of a power interruption (when isolation switch is closed, i.e. not isolating) from the power supplies.

With respect to claims 8 and 9 Humpherys teaches a control circuit (item 175) to receive as input a power status signal (input from comparator), said control circuit to output a control signal (output of 175), said control signal to comprise a switch close

signal if said power status is valid, and a switch open signal if said power status is invalid (col. 5 lines 1-5); and at least one switch to connect to said control circuit, said switch to receive said control signal and at least one of said shelf component signals (carried on bus lines 77) and operate in accordance with said control signal, with said switch to prevent communication of said shelf component signal (isolate the management board) when said switch is in an open state (isolating).

With respect to claims 10 and 11 Humpherys teaches isolating the component signal when the system host is unavailable however does not teach the use of a software signal to be received to signal the control circuit to isolate the component signal. Amicangioli teaches the use of a software timer opening of switch when a failure or expiry of a software timer (col. 4 lines 55-65) to increase the reliability of the network traffic processor deployment. It would have been obvious to one of ordinary skill in the art at the time of the invention to modify Humpherys to include a software input to the control circuit in order to increase the reliability of the network.

With respect to claims 17-18 Humpherys does not describe the signal as a TTL logic control signal. Humpherys teaches the use of PCI communication and signal environment. It would have been obvious to one of ordinary skill in the art at the time of the invention to use TTL logic signals as such type of signals are a well known means of controlling logic level components.

Claim 6 is rejected under 35 U.S.C. 103(a) as being unpatentable over Humpherys et al. (U.S. Pat. No 6,128,682) in view of Amicangioli et al. (U.S. Pat. No. 6,327,242) in view of Edelen et al. (U.S. Pat. No. 6,789,871) Humpherys as modified by

Amicangioli teaches the control circuit and control logic merely as block diagrams and does not describe in detail the types of circuitry utilized in the implementation, It would have been obvious to one of ordinary skill in the art at the time of the invention to use n-channel MOSFET as the use of such solid state circuitry in control logic is commonly implemented in digital switching logic for its low loss and high speed switching characteristics. Edelen also teaches a plurality of switches which are configured to receive a component signal; a control circuit item 340 couple to said plurality of switches and also provides the teaching of dual channel MOSFETs are an obvious substitute for FET relays or other type of switch

Claims 12-13 are rejected under 35 U.S.C. 103(a) as being unpatentable over Humpherys et al. (U.S. Pat. No 6,128,682) in view of Edelen et al. (U.S. Pat. No. 6,789,871)

With respect to claims 12 and 13 Humpherys teaches a switch block (180), with each switch configured to receive a component signal (carried on bus lines 77); a control circuit (item 175) to electrically couple to said switch block, said control circuit to receive a power status signal (col. 5 lines 1-5). Humpherys does not illustrate the use of plural N-channel switches. Edelen also teaches a plurality of switches which are configured to receive a component signal; a control circuit item 340 couple to said plurality of switches and also provides the teaching of dual channel MOSFETs are an obvious substitute for FET electric switching relays or other type of switch therefore It would have been obvious to one of ordinary skill in the art at the time of the invention to

use a dual channel MOSFET in order to reduce line resistance when the when the switch is in a closed state.

Claim 14 is rejected under 35 U.S.C. 103(a) as being unpatentable over Humpherys et al. (U.S. Pat. No 6,128,682) in view of Edelen et al. (U.S. Pat. No. 6,789,871) in view of Amicangioli et al. (U.S. Pat. No 6,327,242) Humpherys as modified by Edelen does not teach the use of software control signal. Humpherys teaches isolating the component signal when the system host is unavailable however does not teach the use of a software signal to be received to signal the control circuit to isolate the component signal. Amicangioli teaches the use of a software timer opening of switch when a failure or expiry of a software timer (col. 4 lines 55-65) to increase the reliability of the network traffic processor deployment. It would have been obvious to one of ordinary skill in the art at the time of the invention to modify Humpherys to include a software input to the control circuit in order to increase the reliability of the network.

Conclusion

Applicant's amendment necessitated the new grounds of rejection presented in this Office action. Accordingly, **THIS ACTION IS MADE FINAL**. See MPEP § 706.07(a). Applicant is reminded of the extension of time policy as set forth in 37 CFR 1.136(a).

A shortened statutory period for reply to this final action is set to expire THREE MONTHS from the mailing date of this action. In the event a first reply is filed within TWO MONTHS of the mailing date of this final action and the advisory action is not mailed until after the end of the THREE-MONTH shortened statutory period, then the shortened statutory period will expire on the date the advisory action is mailed, and any extension fee pursuant to 37 CFR 1.136(a) will be calculated from the mailing date of the advisory action. In no event, however, will the statutory period for reply expire later than SIX MONTHS from the date of this final action.

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Michael Rutland-Wallis whose telephone number is 571-272-5921. The examiner can normally be reached on Monday-Thursday 7:30AM-6:00PM EST.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Michael Sherry can be reached on 571-272-2084. The fax phone number for the organization where this application or proceeding is assigned is 571-273-8300.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free). If you would like assistance from a USPTO Customer Service Representative or access to the automated information system, call 800-786-9199 (IN USA OR CANADA) or 571-272-1000.

MRW

7/24/07

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